Accelerating Yield Improvement !

In this age of lightening fast technological evolution having systems to back-up your Fab investment is critical. Comprehensive Engineering Data Analysis (EDA) is one such system. Empowering your Engineering team to rapidly analyse your Process, Integration and Yield opportunities to drive a World Class Yield Enhancement Roadmap.

Technological Evolution !

Fabs introduce new technologies, processes and products weekly. Aggressively driving change is critical for time to market and maximizing your profit. Introducing a new technology or product, ramping it into High Volume and then sustaining it with high yields, is business as usual.

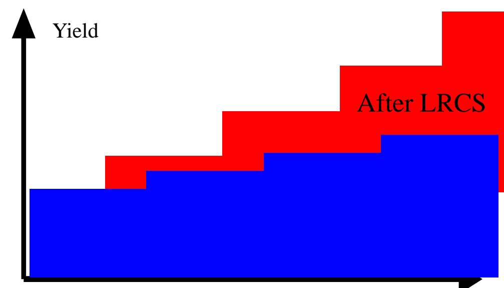
Don't stop short! Protect your investment with a system to turn the wealth of engineering data into real improvements.

Lot Review, Classification and Yield Signature Debug

Exploit your existing EDA system to the full and automatically generate all key reports, maps and charts overnight. Increase the number of Yield opportunities highlighted by the Engineers. Free up their time taken generating routine reports and allow the team to focus on proactive Yield Analysis.

Imagine reviewing all of the previous days test results in 30 minutes after the reports were prepared overnight; Highlighting new yield improvement opportunities or yield loss signatures and starting debug immediately; Using the prepared reports, charts and maps for a first-pass disposition and to narrow down the root cause; Discussing ideas, and reviewing the lot reports real time with the Engineering team; Automatically generating lot lists for the Commonality tools, Material Review Board and OQC; Having an Improvement Action Plan within 12 hours of 1st highlighting the Yield opportunity.

Now imagine every one of your Team having the same Engineering Debug capability!



Benefits $$$

Quicker debug: Assume 30 events (0.5% loss) / QTR. LRCS saves 1 day loss on 15.

More Improvements: Assume 1 extra improvement (0.5% gain) / QTR. 350 DPW & 30K wafers / month

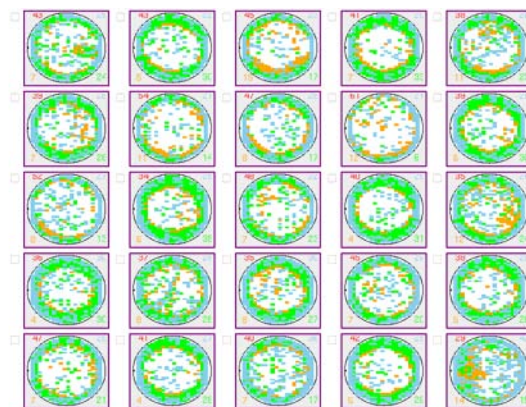
(15*0.5% / 90days) + (1*0.5%) * 350 * 90K * 1$ profit/chip = 367,500 $ / Quarter. (Approx. 0.7 Million USD$ / year extra profit).

Installing LRCS has a guaranteed Return on Investment of less than 6 months.

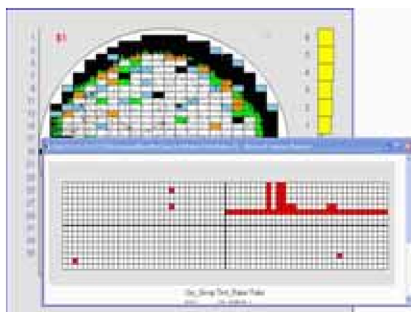
Increasing Opportunities

LRCS is *NOT* a replacement EDA system: Interactive Engineering Data Analysis is essential for day to day problem solving and would be instrumental in following up on the Yield Improvement opportunities highlighted by LRCS. Rather, LRCS is designed to compliment your existing EDA system and maximise its potential. Whilst, at the same time, increasing the analysis productivity of the Engineering Team in generating new Yield Improvement initiatives. Increased Yield initiatives will ultimately lead to Accelerated and Improved Yield benefits.

Reporting All data types: LRCS processes all the usual data sources (Inline, ETest, Wafer Sort, Defect, Final Test) to provide the outputs of choice, with wafer maps being the most logical starting point for Lot review.

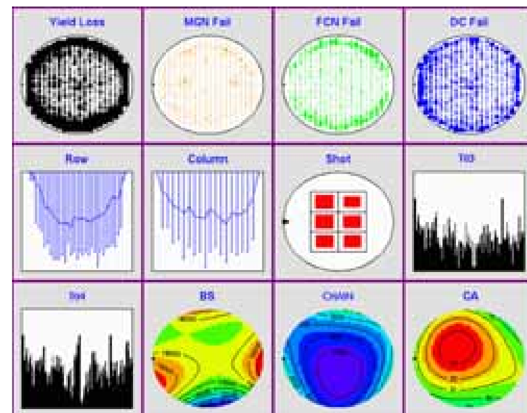


Drilling down to individual wafers or chips:



Different test failures being colour coded, reticle and region performance charts in the legend, and chip level detail if available.

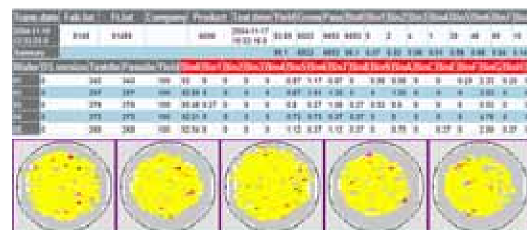
Alternatively the reviewer may prefer to work within the Composite maps view, including row, column shot, DUT and Electrical Test.



Real time debug: After reviewing the maps, the users can change the view to get the specific wafer results from Wafer Sort, Electrical test, In-line or Final Test.

Parameter	distribution	specl	target	spech	average	std	fail	waf01	waf05	waf10	waf15
VTL_0H_An_4.0x0.85		0.53		0.60	0.546	0.081	8	0.0087	0.5549	[illegible]	0.553
VTL_0H_P__10x10.0		-0.64		-0.5	-0.6063	0.009	2	-0.6079	-0.6071	-0.5979	-0.6099
VTS_0H_P__10x0.18		-0.65		-0.36	-0.5034	0.028	4	-0.5526	-0.5008	-0.4889	-0.508
VTS_0H_P__10x0.155		-1.8		-0.1	-0.2763	0.06	2	-0.3639	-0.2609	-0.264	-0.2733
IDS_0H_P__10x0.18		-0.00238		-0.00133	-0.00187	0	4	-0.001793	-0.001843	-0.001844	-0.001894
Delta_LP		-20		30	18.89	6.663	8	13.01	20.33	19.92	20.92
Delta_P18		-20		30	8.750	18.018	5	2.233	8.522	6.954	-0.6774
VTL0H_PLK_10x10.0		-0.54		-0.4	-0.4586	0.069	5	-0.4699	-0.4702	-0.4375	-0.4663
VTS0H_PLK_10x0.21		-0.620		-0.41	-0.4675	0.024	7	-0.4952	-0.4638	-0.4606	-0.4634
SLP_0L_PLK__nom		10		1000	128.8	89.991	16	126.4	185.8	135.1	128.3
VTS0H_PLK_10x0.185		-1.8		-0.1	-0.4026	0.043	6	-0.4481	-0.3935	-0.3842	-0.3991
IDS_H_PLK_10x0.21		-0.00160		-0.0008	-0.001227	0	6	-0.001173	-0.001229	-0.001238	-0.001179
VTL0H_NLK_10x10.0		0.388		0.488	0.4309	0.142	7	0.4304	0.4259	[illegible]	0.3821
VTS0H_NLK_10x0.20		0.338		0.600	0.4299	0.101	10	0.4689	0.4259	0.4339	0.4424

or compare with Defect, Etest or FT Maps,

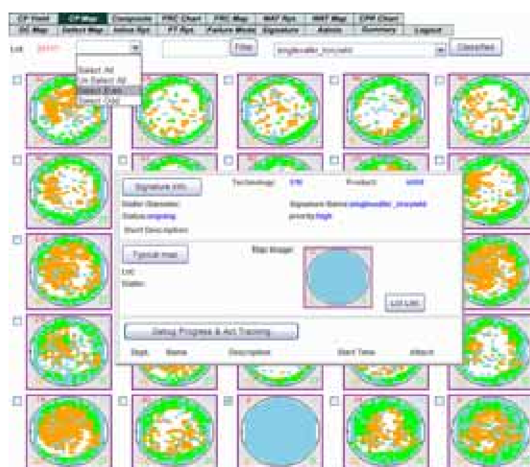


all prepared overnight in advance…

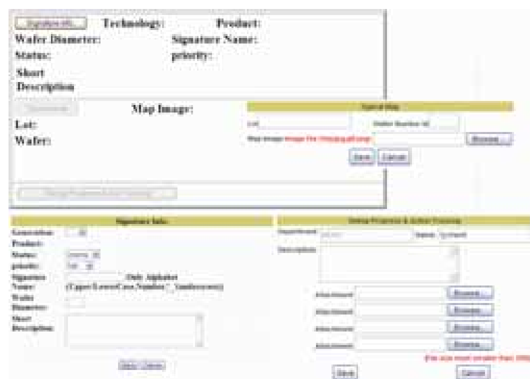
Prioritising Improvements

LRCS *IS* a Yield Management system: The Lot Reports are the basis for the Engineering teams understanding of the health of the Product. However, to improve that Product, the team needs to know the various loss mechanisms, and their impact, to prioritise Improvement activities. This is where LRCS comes into its own, providing Signature classification, Debug workflows and the Knowledge Management.

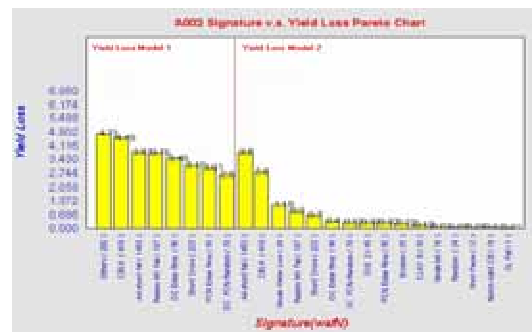
During the Lot Review the User classifies the affected wafers to the known Signatures.



Should a new signature be detected, the User initiates the Signature Knowledge Management system to describe the failure mode, attach maps and any relevant files.

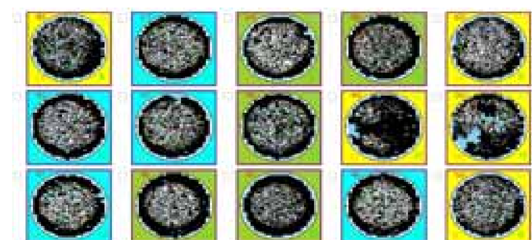


Yield Management: Once several days of production has been classified, the Users can get an overview of the on-going losses.



By drilling down on the Signature, it is possible for the User to review the Signature debug status, update the progress, or obtain a current "affected" lot list for Commonality and Quarantine purposes. However, the most powerful feature of the LRCS Yield Management tools is the Yield Loss Pareto. Within which, each signature is quantified and prioritised for future Improvement.

Experimental Analysis: Of course, once prioritised, a next step is to run experimental lots to investigate the improvement. LRCS completes the process here, simplifying the analysis by <u>automatically</u> splitting (different colours) the reports, maps and charts according to the experimental split plan.



LRCS™ – The System.

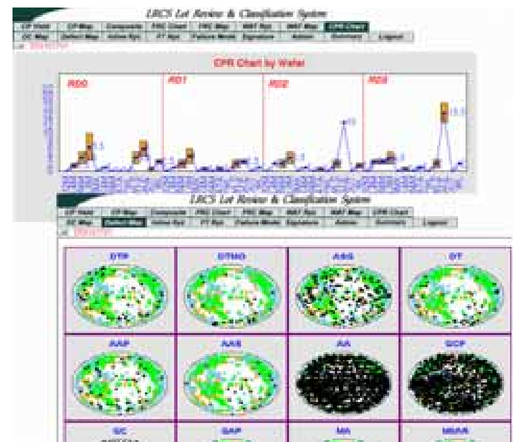
WEB Based: Ease of use, easy deployment; low maintenance; integrated help files are all aspects to appeal to the IT team and Fab engineers alike.

Report content is readily configurable through the User Interface by "Adding" or "Removing" the relevant parameters etc…

The initial query sets the review scene.. Once the criteria are entered, the User then switches between the various reports on-the-fly whilst simultaneously performing wafer classification. The User also has functions to add Lot Comments for all users to see or to Export the data for further analysis.

Remote access: Being a WEB-based application, LRCS can be used in both local and sister Fabs. An Integration engineer can share an experimental lot results with her development counterpart on another continent. The Product Manager at the headquarters can review the latest Signatures with the local Yield Manager. Even foundry customers can be enabled to use the same LRCS system.

Customised Analysis: Customisation is encouraged to meet the Users specific requirements. LRCS can call and run local fab applications, *for example queries into the MES system*. Alternatively, product specific information and reports can be customised, *For example 1st failing vector paretos, Defect maps, Yield Kill Ratio Analysis or Memory fail pattern reports.*



Conclusion: LRCS's Yield Management System with its easy to use menus and prepared reports will greatly improve the Analysis productivity of your Engineering team and the existing EDA system to realise many new Yield Opportunities.

Call now for a demonstration to see how LRCS could work for you in your Fab.

TYNE Systems Corporation
TEL: +886-3-5726781
E-mail: queries@tynesys.com
http://www.tynesys.com